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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Li et al.

Serial No. 09/849,047

Filed: May 4, 2001

For: BURIED LAYER SUBSTRATE ISOLATION IN INTEGRATED CIRCUITS

§ Group Art Unit: 2822
§ Examiner: Lewis, M.
§
§ Atty. Dkt. No. 5298-04500
§ (PM00026)

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April 5, 2004
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Kevin L. Daffer

APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Sir/Madam:

Further to the Notice of Appeal sent via facsimile on February 4, 2004, the Appellant presents this Appeal Brief. The Notice of Appeal was filed following receipt of an Office Action mailed November 5, 2003. The Appellant hereby appeals to the Board of Patent Appeals and Interferences rejections of claims 1-13, 17-21, and 23-25 and respectfully requests that this appeal be considered by the Board.

I. REAL PARTY IN INTEREST

The subject application is owned by Cypress Semiconductor Corporation, a corporation having a place of business at 3901 North First Street, San Jose, CA, 95134.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-28 were originally filed in the present application on May 4, 2001. Claims 14-16, 22, and 26-28 were withdrawn from consideration by the examiner pursuant to a restriction requirement. Claims 1-13, 17-21, and 23-25 stand twice rejected under 35 U.S.C. §§ 102(b) and 103(a) and are the subject of this appeal. A copy of claims 1-13, 17-21, and 23-25, as on appeal, is included in the Appendix attached hereto.

IV. STATUS OF AMENDMENTS

No amendments to the claims have been filed subsequent to their final rejection. Therefore, the Appendix attached hereto reflects the current state of the claims.

V. SUMMARY OF THE INVENTION

Appellant's claimed invention relates to integrated circuit manufacturing, and more particularly to a substrate-isolated transistor (Specification -- page 1, lines 6-7). In particular, an integrated circuit is claimed which includes a transistor formed in a well region of a semiconductor substrate and further includes a buried layer formed within the substrate below the well region. In preferred embodiments, the well region and the semiconductor substrate are of the same conductivity type and the buried layer is of opposite conductivity type than the well region (Specification -- page 3, lines 3-6). In some cases, the integrated circuit may include a doped annular region which extends through the well region to contact the buried layer. In particular, the integrated circuit may include a doped annular region which laterally surrounds the transistor without surrounding other transistors of the integrated circuit. Such a doped annular region is preferably the same conductivity type as the buried layer or, in other words, opposite conductivity type as the well region (Specification -- page 3, lines 10-12). In some embodiments, the buried layer may include a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion. In such cases, the doped annular region may extend past the

well region to contact the second portion of the buried layer (Specification -- pages 3 and 4, lines 29-30 and 1-2, respectively).

In some cases, the integrated circuit may include one or more contact diffusions within the well region which are adapted for making contact to the well region (Specification -- page 12, lines 3-6). In some embodiments, the one or more contact diffusions may include a contact diffusion laterally adjacent to and in contact with a source region of the integrated circuit (Specification -- page 12, lines 10-12). In addition or alternatively, the one or more contact diffusions may include an annular contact diffusion arranged laterally within the doped annular region and laterally surrounding the transistor (Specification -- page 12, lines 12-13). In some embodiments, the integrated circuit may further include a contact to the doped annular region (Specification -- page 13, lines 13-14 and Fig. 7). In such embodiments, the integrated circuit may, in some cases, include metallization adapted to connect the well region and the doped annular region to opposite polarities of a supply voltage (Specification -- page 13 and 14, lines 29-30 and 1-2, respectively). In other embodiments, the integrated circuit may include metallization adapted to connect the well region to one polarity of a supply voltage for the integrated circuit, while precluding connection of the doped annular region to the other polarity of the supply voltage (Specification -- page 14, lines 12-14). For example, the integrated circuit may, in some embodiments, include metallization adapted to connect the well region and doped annular region to the same polarity of the supply voltage (Specification -- page 14, lines 16-18). Alternatively, the metallization may be adapted to preclude connection of the doped annular region to any supply voltage of the integrated circuit (Specification -- page 14, lines 25-27).

In embodiments in which buried layer includes laterally spaced first and second portions, the integrated circuit may include a depletion region bridging the separation between the first and second portions of the buried layer. In embodiments in which the well region and the doped annular region are connected to opposite polarities of the supply voltage, the depletion region may bridge the separation at a lower end of the buried layer (Specification -- page 15, lines 21-25). Such a depletion region may serve to increase noise isolation between the well region and the substrate (Specification -- page 15, lines 28-29). In general, the first and second portions of the buried layer may be separated by a distance of less than about 5 microns and, in some embodiments, specifically by a distance of approximately 1.2 microns (Specification -- page 15, lines 16-21). In any case, the integrated circuit may include an annular dielectric isolation region laterally surrounding the transistor in some embodiments (Specification -- page 10, lines 9-10). In addition, the transistor may be an output transistor for the integrated circuit in some

cases (Specification -- page 3, lines 8-9). In such embodiments, the integrated circuit may further include one or more analog circuit portions (Specification -- page 3, lines 14-15).

VI. ISSUES

1. Whether claims 1-3, 6-9 and 11 are unpatentable under 35 U.S.C. § 102(b) by U.S. Patent No. 4,862,242 Wildi et al. (hereinafter referred to as "Wildi").

2. Whether claims 4, 5, 10, 17-19 and 23-25 are unpatentable under 35 U.S.C § 103(a) by Wildi.

3. Whether claims 12, 13, 20 and 21 are unpatentable under 35 U.S.C § 103(a) by Wildi in view of U.S. Patent No. 6,051,868 Watanabe et al. (hereinafter referred to as "Watanabe").

VII. GROUPING OF CLAIMS

Claims 1, 3, 12 and 13 (Group I) stand or fall together.
Claims 2, 6, 7, 9 and 10 (Group II) stand or fall together.
Claim 4 (Group III) stands or falls alone.
Claim 5 (Group IV) stands or falls alone.
Claim 8 (Group V) stands or falls alone.
Claim 11 (Group VI) stands or falls alone.
Claims 17-21 (Group VII) stand or fall together.
Claims 23 and 25 (Group VIII) stand or fall together.
Claim 24 (Group IX) stands or falls alone.

The reasons why the nine groups of claims are believed to be separately patentable are explained below in the appropriate parts of the Argument.

VIII. ARGUMENT

Mixed signal, or mixed mode, integrated circuits which include analog and digital circuit portions are becoming increasingly popular. For example, many wireless communications applications involve mixed signal integrated circuits. Noise problems can arise in such circuits because analog circuit

portions tend to be noise-sensitive, while relatively high-power switching transistors, such as output transistors associated with the digital circuit portions, tend to generate noise. In a mixed signal circuit, noise from an output transistor can be coupled to an analog circuit portion through the semiconductor substrate shared by the entire integrated circuit. *See,* Specification: page 1.

The invention recited in claims 1-13, 17-21, and 23-25 includes integrated circuits which advantageously reduce noise coupling between output transistors and analog circuit portions. In particular, the integrated circuits of the presently claimed case provide substrate isolation for noise-prone transistors. Consequently, the performance of analog circuit portions included in the same semiconductor die may be improved. The integrated circuits of the presently claimed case include transistors formed within wells having the same conductivity as the semiconductor substrate and include buried layers having a conductivity type opposite to that of overlying wells. In some cases, a doped annular region having the same conductivity type as a buried layer may be formed to laterally surround the noise-prone transistor and contact the buried layer. In an embodiment, the integrated circuit may include metallization configured to connect opposite-polarity supply voltages to the well and doped annular region. Alternatively, the metallization may be adapted to connect the doped annular region to the same voltage polarity as the well. In yet other embodiments, the metallization may be adapted to leave the doped annular region floating. In still a further embodiment, the buried layer may be formed in two portions: a central portion underlying the transistor, and a separate portion spaced apart from and laterally surrounding the central portion. The doped annular region surrounding the transistor may contact the outer portion of the buried layer. In such an embodiment, the central portion of the buried layer remains electrically "floating" regardless of the voltage applied by a topside contact to the doped annular region. *See,* Specification: pages 3-4.

ISSUE 1 ARGUMENTS

A. Patentability of Group I Claims 1 and 3

1. Wildi fails to disclose an integrated circuit having a buried layer with a first portion underlying a transistor and a second portion spaced apart from and laterally surrounding the first portion.

Claim 1 recites in part: "[a]n integrated circuit, comprising: a transistor formed in a well region of a semiconductor substrate ... and a buried layer formed within the substrate below the well region ... wherein the buried layer includes a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion." The Office Action cites buried layer 318 in Fig. 3 of Wildi as serving as the buried layer recited in claim 1. As shown in Fig. 3 of Wildi, buried layer 318 is a contiguous layer arranged below n-channel MOSFET 350. Buried layer 318 does not include any additional portions spaced apart and laterally surrounding the contiguous layer. Consequently, buried layer 318 fails to meet the limitations of the buried layer recited in claim 1. Furthermore, Wildi fails to provide a buried layer having distinct portions spaced apart from each other in the embodiments discussed in reference to Figs. 1, 2 and 4-6. Consequently, it is asserted that Wildi does not anticipate the limitations of claim 1.

2. None of the various doped regions included within the topography taught by Wildi can serve as a second portion of a buried layer as defined by the limitations of claim 1.

Fig. 3 of Wildi shows buried layer 318 arranged underneath n-channel MOSFET 350. Consequently, buried layer 318 may serve as the first portion of the buried layer as recited in claim 1. Although Wildi teaches various doped regions above, below and laterally adjacent to buried layer 318, none of such layers can serve as a second portion of the buried layer as defined by the limitations of claim 1. In particular, none of high voltage region 316, portion 328 of epitaxial layer 304, ground region 326, and the outermost portion of epitaxial layer 304 laterally surrounding ground region 326 are spaced apart and laterally surround buried layer 318. In addition, none of high voltage region 316, portion 328 of epitaxial layer 304, ground region 326, and the outermost portion of epitaxial layer 304 are buried layers and, therefore, cannot serve as the second portion of buried layer 318.

As shown in Fig. 3, Wildi provides high voltage region 316 above and in alignment with the peripheral edges of buried layer 318. Consequently, high voltage region 316 is not spaced apart from buried layer 318 nor does high voltage region 316 laterally surround buried layer 318. In addition, high voltage region 316 extends above buried layer 318 to the surface of epitaxial layer 304 and, therefore, is not a buried layer. Similarly, portion 328 of epitaxial layer 304, ground region 326, and the outermost portion of epitaxial layer 304 laterally surrounding ground region 326 extend to the surface of epitaxial layer 304 and, therefore, are not buried layers. In addition, portion 328 and the outermost portion of epitaxial layer 304 include different concentrations of dopants than buried layer

318. In particular, portion 328 and the outermost portion of epitaxial layer 304 include low concentrations of dopants as denoted by the N- reference, while buried layer 318 includes a high concentration of dopants as denoted by the N+ reference. Consequently, portion 328 and the outermost portion of epitaxial layer 304 cannot be considered portions of buried layer 318. Moreover, ground region 326 is doped with the opposite conductivity type as buried layer 318 and, therefore, cannot be considered a portion of buried layer 318 either. Such a lack of teaching within the embodiment discussed in reference to Fig. 3 cannot be overcome by the embodiments discussed in reference to Figs. 1, 2 and 4-6, since the doped regions therein are formed having substantially similar configurations as the doped regions described in reference to Fig. 3. Consequently, none of the various doped regions taught by Wildi can serve as the second portion of the buried layer recited in claim 1.

3. The Examiner has failed to provide sufficient grounds for the rejection of claim 1.

The Examiner states on page 7 of the Office Action that the Applicant's arguments filed September 29, 2003 stating that the prior art does not disclose a buried layer with a first portion underlying a transistor and a second portion spaced apart from and laterally surrounding the first portion are not persuasive. In particular, the Examiner maintains that "Wildi discloses a buried layer where the first portion underlies the transistor and the second portion of the buried layer is spaced apart from and laterally surrounding the first portion." (Office Action, page 7). The Office Action, however, does not distinguish what portion of wafer 300 in Fig. 3 of Wildi is interpreted to serve as the second portion of the claimed buried layer. As noted above, none of the various doped regions taught by Wildi are spaced apart and laterally surround buried layer 318. Consequently, none of the various doped regions taught by Wildi can serve as the second portion of the buried layer recited in claim 1. It is, therefore, asserted that the Examiner has failed to provide sufficient grounds for the rejection of claim 1.

Conclusion

As explained in Arguments 1-2 above, at least some limitations of independent claim 1 are not disclosed by Wildi. Consequently, independent claim 1 is not anticipated by Wildi. Since claim 3 is dependent from claim 1, claim 3 is not anticipated by Wildi for at least the same reasons as that claim. In addition, it is asserted that the Examiner has failed to provide sufficient grounds for the rejection of claim

1. Accordingly, the § 102(b) rejection of Group I claims 1 and 3 in light of Wildi is asserted to be erroneous.

B. Patentability of Group II Claims 2, 6, 7 and 9

Since claims 2, 6, 7 and 9 of Group II are dependent from claim 1, the arguments presented above for the patentability of Group I claims 1 and 3 in light of Wildi apply equally to claims 2, 6, 7 and 9 and are herein incorporated by reference. Claim 2 specifies that the integrated circuit includes a doped annular region which contacts the second portion of the buried layer. This limitation makes claim 2 separately patentable over the cited art, as described in more detail below.

1. Wildi fails to disclose an integrated circuit having a doped annular region contacting a portion of a buried layer, which is spaced apart and laterally surrounds another portion of the buried layer underlying a transistor.

Claim 2 recites, "The integrated circuit as recited in claim 1, further comprising a doped annular region of opposite conductivity type as the well region and extending past the well region to contact the second portion of the buried layer." As noted above in the arguments traversing the § 102(b) rejection of Group I claims 1 and 3, Wildi does not disclose a buried layer with two distinct portions spaced apart from each other, much less a buried layer with one portion laterally surrounding another portion. As such, Wildi does not teach a doped annular region in contact with a portion of a buried layer which is spaced apart and laterally surrounds another portion of the buried layer as defined in claim 2. It is, therefore, asserted that Wildi does not anticipate the limitations of claim 2.

2. The high voltage region taught in Wildi cannot serve as the doped annular region recited in claim 2.

The Office Action cites high voltage region 316 illustrated in Fig. 3 of Wildi as serving as the doped annular region recited in claim 2. As shown in Fig. 3, high voltage region 316 is in contact with buried layer 318, but, as noted above, buried layer 318 does not include distinct portions spaced apart from each other. Consequently, high voltage region 316 does not contact a second portion of buried layer 318 as specified for the doped annular region recited in claim 2. Consequently, the citation of high voltage region 316 to be equivalent to the claimed doped annular region is asserted to be erroneous.

Conclusion

As explained in Arguments 1 and 2 above, at least some limitations of dependent claim 2 are not disclosed by Wildi. Consequently, dependent claim 2 is not anticipated by Wildi. Since claims 6, 7 and 9 are dependent from claim 2, claims 6, 7 and 9 are not anticipated by Wildi for at least the same reasons as that claim. Accordingly, the § 102(b) rejection of Group II claims 2, 6, 7 and 9 in light of Wildi is asserted to be erroneous.

C. Patentability of Group V Claim 8

Since claim 8 of Group V is dependent from claims 1, 2 and 6, the arguments presented above for the patentability of Group I claims 1 and 3 and the arguments presented for the patentability of Group II claims 2, 6, 7 and 9 in light of Wildi apply equally to claim 8 and are herein incorporated by reference. Claim 8 specifies that the one or more contact diffusions recited in claim 6 include an annular contact diffusion region surrounding the transistor recited in claim 1. This limitation makes claim 8 separately patentable over the cited art, as described in more detail below.

1. Wildi fails to disclose an integrated circuit having an annular contact diffusion region within a well region in which the circuit is formed.

Claim 8 recites, "The integrated circuit as recited in claim 6, wherein said one or more contact diffusions comprises an annular contact diffusion arranged laterally within the doped annular region and laterally surrounding the transistor." Dependent claim 6 specifies the one or more contact diffusions are formed within the well region recited in independent claim 1. Claim 1 specifies that the well region is of the same conductivity type as the substrate. In context with such a limitation of the well region, it is presumed that p channel threshold control region 351 of Wildi may serve as the claimed well region. As shown in Fig. 3 of Wildi, wafer 300 includes source and drain regions 352 and 354 and P+ region 364 within p channel threshold control region 351. None of such regions, however, are shown as annular nor laterally surround n-channel MOSFET 350. Rather, each of the regions extends along one of the two sides of gate 360 as an elongated channel. Consequently, Fig. 3 of Wildi fails to disclose the limitations of claim 8.

Wildi does illustrate in Fig. 6 bipolar transistor 650 including P+ collector region 654 laterally surrounding emitter electrode 656, but such a configuration does not meet the limitations of claim 8. In particular, P+ collector region 654 serves as a portion of bipolar transistor 650 and, therefore, cannot laterally surround the transistor. Furthermore, bipolar transistor 650 is not formed within a well region having the same conductivity type as substrate 602. In particular, P+ collector region 654 is formed within N- device region 620 without an additional doped region therebetween. Consequently, Fig. 6 of Wildi does not anticipate the limitations of claim 8.

2. There is no motivation within Wildi to teach an integrated circuit having an annular contact diffusion region within a well region in which the circuit is formed.

Not only does Figs. 3 and 6 not teach the limitations of claim 8, there is no motivation within Wildi to combine the components of Figs. 3 and 6 to teach the limitations of claim 8. In particular, there is no motivation to modify Fig. 3 to include annular P+ collector region 654 within p channel threshold control region 351. In addition, there is no motivation to modify Fig. 6 to include a well region having the same conductivity type as substrate 602 nor include an annular contact diffusion region around the entirety of bipolar transistor 650. Figs. 3 and 6 illustrate isolation techniques for two different types of transistors, namely an n-channel MOSFET and a bipolar transistor. Each of such transistors necessitates different layouts, concentrations and conductivity types of diffusion regions for their operation. Modifying such diffusion regions may alter the operation of the transistors. If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); MPEP 2143.01. Consequently, there is no motivation to modify within Wildi to teach an integrated circuit having an annular contact diffusion region within a well region in which the circuit is formed.

Conclusion

As explained in Arguments 1 and 2 above, the limitation of dependent claim 8 is not taught or suggested by Wildi. Furthermore, there is no motivation within Wildi to teach the limitations of claim 8. Consequently, dependent claim 8 is not taught or suggested by Wildi. Accordingly, the § 102(b) rejection of Group V claim 8 in light of Wildi is asserted to be erroneous.

D. Patentability of Group VII Claim 11

Since claim 11 of Group VI is dependent from claims 1 and 2, the arguments presented above for the patentability of Group I claims 1 and 3 and the arguments presented for the patentability of Group II claims 2, 6, 7 and 9 in light of Wildi apply equally to claim 11 and are herein incorporated by reference. Claim 11 specifies that the integrated circuit further includes an annular dielectric isolation region laterally surrounding the transistor. This limitation makes claim 11 separately patentable over the cited art, as described in more detail below.

1. Wildi fails to disclose an integrated circuit having an annular dielectric isolation region laterally surrounding a transistor.

Claim 11 recites, "The integrated circuit as recited in claim 2, further comprising an annular dielectric isolation region laterally surrounding the transistor." The Office Action references Fig. 3 of Wildi as teaching an integrated circuit having an annular dielectric isolation region laterally surrounding a transistor. There is, however, no illustration of an isolation region included within Fig. 3, much less one that laterally surrounds n-channel MOSFET 350. Rather, Wildi teaches various doped regions of epitaxial layer 304 surrounding n-channel MOSFET 350. In addition, there is no teaching or suggestion in the text of Wildi of including a dielectric isolation region within wafer 300 depicted in Fig. 3 or in any of the topographies depicted and described in reference to Figs. 1, 2 and 4-6. Consequently, Wildi fails to anticipate the limitations of claim 11.

2. There is no motivation to modify the wafers provided in Wildi to include an annular dielectric isolation region which laterally surrounds a transistor.

The objective of Wildi is "... to provide a semiconductor wafer incorporating an electrically isolated semiconductor device with such electrical isolation achieved through the use of [a] semiconductor material." (Wildi, column 1, lines 45-49). In fact, Wildi specifically "... describes various embodiments of a semiconductor wafer incorporating semiconductor devices that are electrically isolated from a substrate of the wafer and from each other by semiconductor material[s] rather than dielectric material[s] as in the prior art." (Wildi, column 8, lines 3-11). Consequently, there is no motivation to modify the wafers provided in Wildi to include a dielectric isolation region which laterally surrounds a transistor.

Conclusion

As explained in Arguments 1 and 2 above, the limitation of dependent claim 11 is not taught or suggested by Wildi. In addition, there is no motivation to modify Wildi to teach the limitations of claim 11. Consequently, dependent claim 11 is asserted to be patentably distinct over Wildi. Accordingly, the § 102(b) rejection of Group VII claim 11 in light of Wildi is asserted to be erroneous.

ISSUE 2 ARGUMENTS

A. Patentability of Group III Claim 4

Since claim 4 of Group III is dependent from claim 1, the arguments presented above for the patentability of Group I claims 1 and 3 in light of Wildi apply equally to claim 4 and are herein incorporated by reference. Claim 4 specifies that the distance between the first and second portions of the buried layer recited in claim 1 is less than approximately 5 microns. This limitation makes claim 4 separately patentable over the cited art, as described in more detail below.

1. Wildi fails to teach, suggest or provide any motivation to teach an integrated circuit having a buried layer with two distinct portions spaced apart by less than approximately 5 microns.

Claim 4 recites, "The integrated circuit as recited in claim 1, wherein the first and second portions of the buried layer are separated by a distance of less than about 5 microns." The Office Action admittedly states that Wildi fails to disclose the limitations of claim 4. In fact, as noted above, Wildi fails to disclose a buried layer with distinct portions spaced apart from each other. Consequently, there is no motivation for Wildi to teach the limitations of claim 4. To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03.

2. The Applicant has established the criticality of fabricating buried layers portions with small separation distances.

The Office Action states that "... the applicant has not established the critical nature of the dimension of less than 5 microns..." (Office Action, page 4). Such a statement is traversed, however, since the Specification clearly teaches the criticality of fabricating buried layer portions with such small separation

distances to promote "pinching off" the lower end of the buried layer. In particular, the Specification states:

> The spacing needed between two such openings in the masking layer depends on the final separation of the buried layer portions desired, allowing for diffusion during processing. The final desired separation in turn depends on details, such as doping levels, of the particular fabrication process used. In some embodiments, for example, a masking layer spacing of about 2.1 microns may result in a post-processing separation of about 1.2 microns between the buried layer portions. In an embodiment, the separation between the buried layer portions after processing is such that the oppositely-doped region between the portions is "pinched off" during operation by depletion regions at the lower end of the buried layer, while retaining some undepleted material at the upper end of the buried layer. Such an embodiment is illustrated using dashed-line depletion region boundaries 90 in Fig. 8. The buried layer may separation be designed so that the "pinch-off" occurs when outer buried layer portion 88 is connected to VCC (for an n+ buried layer). This "pinch-off" may reduce substantially the coupling of noise generated by n-channel transistor 63 to p-type substrate 46. (Specification – page 15, lines 16-29)

As such, it is asserted that the Applicant has established the critical nature of the dimensions specified in claim 4.

Conclusion

As explained in Arguments 1 and 2 above, the limitation of dependent claim 4 is not taught or suggested by Wildi. In addition, it is asserted that the Applicant has established the criticality of fabricating buried layers portions with small separation distances. Consequently, dependent claim 4 is asserted to be patentably distinct over Wildi. Accordingly, the § 103(a) rejection of Group III claim 4 in light of Wildi is asserted to be erroneous.

B. Patentability of Group IV Claim 5

Since claim 5 of Group IV is dependent from claims 1 and 4, the arguments presented above for the patentability of Group I claims 1 and 3 and Group III claim 4 in light of Wildi apply equally to claim 5 and are herein incorporated by reference. Claim 5 specifies that the distance between the first and second portions of the buried layer recited in claim 1 is approximately 1.2 microns. This limitation makes claim 5 separately patentable over the cited art, as described in more detail below.

1. Wildi fails to teach, suggest or provide any motivation to teach an integrated circuit having a buried layer with two distinct portions spaced apart by approximately 1.2 microns.

Claim 5 recites, "The integrated circuit as recited in claim 4, wherein the first and second portions of the buried layer are separated by a distance of approximately 1.2 microns." The Office Action admittedly states that Wildi fails to disclose the limitations of claim 5. As noted above, Wildi fails to disclose a buried layer with distinct portions spaced apart from each other. Consequently, there is no motivation for Wildi to teach the limitations of claim 5.

2. The Applicant has established the criticality of fabricating buried layers portions with small separation distances.

It has been clearly shown in reference to the arguments regarding the patentability of dependent claim 4 that the Applicant has established the critical nature of the dimensions specified in claim 5. Consequently, the basis for rejection cited in the Office Action stating the Applicant has not established the critical nature of the dimension of approximately 1.2 microns is erroneous.

Conclusion

As explained in Arguments 1 and 2 above, the limitation of dependent claim 5 is not taught or suggested by Wildi. In addition, it is asserted that the Applicant has established the criticality of fabricating buried layers portions with small separation distances. Consequently, dependent claim 5 is asserted to be patentably distinct over Wildi. Accordingly, the § 103(a) rejection of Group IV claim 5 in light of Wildi is asserted to be erroneous.

C. Patentability of Group II Claim 10

Because claim 10 of Group II is dependent from claims 1, 2, 6 and 9, the arguments presented above for the patentability of Group I claims 1 and 3 and the patentability of Group II claims 2, 6, 7 and 9 in light of Wildi apply equally to claim 10 and are herein incorporated by reference. Accordingly, the §103(a) rejection of Group II claim 10 is asserted to be erroneous.

D. Patentability of Group VII Claims 17-19

1. Wildi does not teach, suggest or provide any motivation to teach an integrated circuit having a transistor formed in a well region of a semiconductor substrate and a doped annular region extending through the well region, wherein the well region is of the same conductivity type as the substrate.

Independent claim 17 recites, in part:

> An integrated circuit, comprising: a transistor formed in a well region of a semiconductor substrate, wherein the well region is of the same conductivity type as the substrate; a buried layer formed within the substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region; a doped annular region extending through the well region to contact the buried layer, wherein the doped annular region is of the same conductivity type as the buried layer...

The Office Action cites Fig. 3 of Wildi as teaching the limitations of claim 17 and specifically cites high voltage region 116 as serving as the claimed doped annular region. High voltage region 116, however, does not extend through a region which is of the same conductivity type as substrate 302 and, therefore, does not meet the limitations which define the doped annular region of claim 17. Rather, high voltage region 116 separates portions 120 and 128 of epitaxial layer 104 which has opposite conductivity to substrate 302. Consequently, high voltage region 116 cannot serve as the doped annular region included in claim 17.

In addition, Wildi fails to teach any doped annular region extending through channel threshold control region 351, which is of the same conductivity as substrate 302 and, therefore, may serve as the claimed well region. In particular, the only doped regions included within channel threshold control region 351 are source region 352, drain region 354 and p+ region 364, none of which are annular or extend through well region 351. It is, therefore, asserted that Wildi does not teach or suggest the limitations of claim 17. Without any teaching or suggestion to teach the limitations of claim 17, there is no motivation within Wildi to teach the integrated circuit recited in claim 17. To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03.

Conclusion

As explained in Argument 1 above, there is no teaching, suggestion or motivation to teach the limitation of independent claim 17 within Wildi. Consequently, claim 17 is asserted to be patentably distinct over Wildi. Since claims 18 and 19 are dependent from claim 17, claims 18 and 19 are patentably distinct from Wildi for at least the same reasons as that claim. Accordingly, the § 103(a) rejection of Group VII claims 17-19 in light of Wildi is asserted to be erroneous.

E. Patentability of Group VIII Claims 23 and 25

Since claim 23 of Group VIII is dependent from claims 1, 2, 6, 9 and 10, the arguments presented above for the patentability of Group I claims 1 and 3 and the patentability of Group II claims 2, 6, 7, 9, 10 in light of Wildi apply equally to claim 23 and are herein incorporated by reference. Claim 23 specifies the inclusion of a depletion region between the first and second portions of the buried layer recited in claim 1. This limitation makes claim 23 separately patentable over the cited art, as described in more detail below.

1. Wildi fails to teach or suggest an integrated circuit having a depletion region between two distinct portions of a buried layer that are spaced apart from each other.

Claim 23 recites, "The integrated circuit as recited in claim 10, further comprising a depletion region bridging the separation between the first and second portions of the buried layer, during times in which the well region and the doped annular region are connected to said opposite polarities of the supply voltage." As noted above in the arguments traversing the § 102(b) rejection of Group I claims 1 and 3, Wildi does not disclose a buried layer with two distinct portions spaced apart from each other. As such, Wildi does not teach a depletion region between two portions of a buried layer. It is, therefore, asserted that Wildi does not teach or suggest the limitations of claim 23.

2. The integrated circuit provided by Wildi is specifically designed to prevent the formation of depletion regions.

Wildi teaches, "Buried layer 118 underlies N+ high voltage region and the entirety of device region 120 and electrically isolates semiconductor resistor 106 from P-substrate 102, ... preventing depletion region reach-through between resistor 106 and substrate 102. This is accomplished by N+ buried layer 118 since it is highly doped and accordingly resists depletion of electrons vertically

therethrough." (Wildi, column 3, lines 25-33). Wildi teaches that the prevention of forming such regions may be applicable to the embodiment described in reference to Fig. 3, in which n-channel MOSFET 350 is isolated from substrate 302. "Wafer 300 is essentially similar to wafer 100 (FIG. 1) except for containing a different semiconductor device in its high voltage tub 314. Accordingly, like parts as between wafers 100 and 300 have identical reference numerals except for the first digit of the reference numerals." (Wildi, column 5, lines 58-63). Consequently, not only does Wildi not teach the inclusion of a depletion region with an integrated circuit, Wildi specifically teaches that the formation of depletion regions are prevented in the integrated circuit design described therein. Consequently, there is no motivation within Wildi to teach the limitations of claim 23.

Conclusion

As explained in Arguments 1 and 2 above, the limitation of dependent claim 23 is not taught or suggested by Wildi. In addition, there is no motivation within Wildi to teach the limitations of claim 23. Consequently, dependent claim 23 is asserted to be patentably distinct over Wildi. Since claim 25 is dependent from claim 23, claim 23 is patentably distinct from Wildi for at least the same reasons as that claim. Accordingly, the § 103(a) rejection of Group VIII claims 23 and 25 in light of Wildi is asserted to be erroneous.

F. Patentability of Group IX Claim 24

Since claim 24 of Group IX is dependent from claims 1, 2, 6, 9, 10 and 23, the arguments presented above for the patentability of Group I claims 1 and 3, Group II claims 2, 6, 7, 9 and 10 and Group VIII claim 23 in light of Wildi apply equally to claim 24 and are herein incorporated by reference. Claim 24 specifies the depletion region bridges the separation of the first and second portions at a lower end of the buried layer. This limitation makes claim 24 separately patentable over the cited art, as described in more detail below.

1. Wildi fails to teach, suggest or provide motivation to teach an integrated circuit having a depletion region which bridges a lower end of a separation between two distinct portions of a buried layer.

Claim 24 recites, "The integrated circuit as recited in claim 23, wherein the depletion region bridges the separation at a lower end of the buried layer." As noted above in the arguments traversing the § 103(a) rejection of Group VIII claim 23, Wildi does not teach or suggest a depletion

region between two portions of a buried layer. As such, Wildi does not teach or suggest a depletion region which bridges a lower end between two portions of a buried layer. In addition, there is no teaching or suggestion of how a depletion region could be formed to bridge a lower end portion of a separation between buried layer portions. It is, therefore, asserted that Wildi does not teach, suggest or provide motivation to teach the limitations of claim 24.

Conclusion

As explained in Argument 1 above, there is no teaching, suggestion or motivation to teach the limitation of independent claim 24 within Wildi. Consequently, claim 24 is asserted to be patentably distinct over Wildi. Accordingly, the § 103(a) rejection of Group IX claim 24 in light of Wildi is asserted to be erroneous.

ISSUE 3 ARGUMENTS

A. Patentability of Group I Claims 12 and 13

Because claims 12 and 13 of Group I are dependent from claim 1, the arguments presented above traversing the § 102(b) rejection of Group I claims 1 and 3 in light of Wildi apply equally to claims 12 and 13 and are herein incorporated by reference. Accordingly, the §103(a) rejection of Group I claims 12 and 13 are asserted to be erroneous.

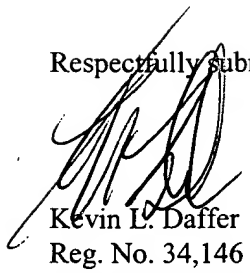
B. Patentability of Group IX Claims 20 and 21

Because claims 20 and 21 of Group VII are dependent from claim 17, the arguments presented above traversing the § 103(a) rejection of Group VII claims 17-19 in light of Wildi apply equally to claims 20 and 21 and are herein incorporated by reference. Accordingly, the §103(a) rejection of Group VII claims 20 and 21 are asserted to be erroneous.

IX. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-13, 17-21, and 23-25 was erroneous, and reversal of the decision is respectfully requested.

Respectfully submitted,



Kevin L. Daffer
Reg. No. 34,146
Attorney for Appellant

Conley, Rose & Tayon, P.C.
P.O. Box 398
Austin, TX 78767-0398
Date: April 5, 2004
MEL

X. APPENDIX

The present claims on appeal are as follows.

1. An integrated circuit, comprising:

a transistor formed in a well region of a semiconductor substrate, wherein the well region and the semiconductor substrate are of the same conductivity type; and

a buried layer formed within the substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region, and wherein the buried layer includes a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion.

2. The integrated circuit as recited in claim 1, further comprising a doped annular region of opposite conductivity type as the well region and extending past the well region to contact the second portion of the buried layer.

3. The integrated circuit as recited in claim 2, wherein the doped annular region laterally surrounds the transistor without surrounding other transistors of the integrated circuit.

4. The integrated circuit as recited in claim 1, wherein the first and second portions of the buried layer are separated by a distance of less than about 5 microns.

5. The integrated circuit as recited in claim 4, wherein the first and second portions of the buried layer are separated by a distance of approximately 1.2 microns.

6. The integrated circuit as recited in claim 2, further comprising one or more contact diffusions within the well region adapted for making contact to the well region.

7. The integrated circuit as recited in claim 6, wherein said one or more contact diffusions comprises a contact diffusion laterally adjacent to and in contact with the source region.

8. The integrated circuit as recited in claim 6, wherein said one or more contact diffusions comprises an annular contact diffusion arranged laterally within the doped annular region and laterally surrounding the transistor.

9. The integrated circuit as recited in claim 6, further comprising a contact to the doped annular region.

10. The integrated circuit as recited in claim 9, further comprising metallization adapted to connect the well region and the doped annular region to opposite polarities of a supply voltage.

11. The integrated circuit as recited in claim 2, further comprising an annular dielectric isolation region laterally surrounding the transistor.

12. The integrated circuit as recited in claim 1, wherein the transistor is an output transistor for the integrated circuit.

13. The integrated circuit as recited in claim 1, further comprising one or more analog circuit portions.

17. An integrated circuit, comprising:

a transistor formed in a well region of a semiconductor substrate, wherein the well region is of the same conductivity type as the substrate;

a buried layer formed within the substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region;

a doped annular region extending through the well region to contact the buried layer, wherein the doped annular region is of the same conductivity type as the buried layer; and

metallization adapted to connect the well region to one polarity of a supply voltage for the integrated circuit, while precluding connection of the doped annular region to the other polarity of the supply voltage.

18. The integrated circuit as recited in claim 17, wherein the metallization is adapted to preclude connection of the doped annular region to any supply voltage of the integrated circuit.

19. The integrated circuit as recited in claim 17, wherein the metallization is adapted to connect the well region and doped annular region to the same polarity of the supply voltage.

20. The integrated circuit as recited in claim 17, wherein the transistor is an output transistor of the integrated circuit.

21. The integrated circuit as recited in claim 17, further comprising one or more analog circuit portions.

23. The integrated circuit as recited in claim 10, further comprising a depletion region bridging the separation between the first and second portions of the buried layer, during times in which the well region and the doped annular region are connected to said opposite polarities of the supply voltage.

24. The integrated circuit as recited in claim 23, wherein the depletion region bridges the separation at a lower end of the buried layer.

25. The integrated circuit as recited in claim 23, wherein the depletion region increases noise isolation between the well region and the substrate.